SYSTEM FOR HANDLING MEMORY REQUESTS AND METHOD THEREOF

ABSTRACT OF THE DISCLOSURE

A system and methods are shown for handling multiple target memory requests. Memory read requests generated by a peripheral component interconnect (PCI) client are received by a PCI bus controller. The PCI bus controller passes the memory request to a memory controller used to access main memory. The memory controller passes the memory request to a bus interface unit used to access cache memory and a processor. The bus interface unit determines if cache memory can be used to provide the data associated with the PCI client's memory request. While the bus interface unit determines if cache memory may be used, the memory controller continues to process the memory request to main memory. If cache memory can be used, the bus interface unit provides the data to the PCI client and sends a notification to the memory controller. The memory controller identifies the memory request, or returned data associated with the request, and discards it to ensure no data is returned to the bus controller from the memory controller. Once the data is received from the bus interface unit, the bus controller is free to send new memory read requests to the memory controller.